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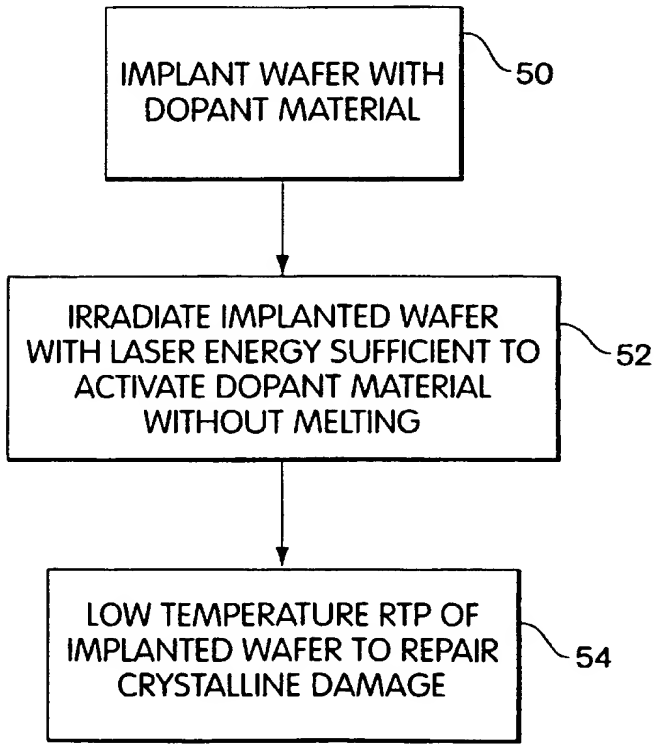
(54) Title: METHOD OF FORMING ULTRASHALLOW JUNCTIONS BY LASER ANNEALING AND RAPID THERMAL ANNEALING



(57) Abstract: Methods are provided for thermal processing of a semiconductor wafer that contains a dopant material. The wafer is irradiated with laser energy sufficient to activate the dopant material without melting the wafer. In addition, rapid thermal annealing of the wafer is performed at relatively low temperature to repair crystalline damage. The dopant activation is achieved with no measurable diffusion. The low temperature rapid thermal anneal repairs crystalline damage, so that devices have good mobilities and low leakage currents.

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METHOD OF FORMING ULTRASHALLOW JUNCTIONS BY LASER ANNEALING AND RAPID THERMAL ANNEALING

Cross-Reference to Related Application

This application claims the benefit of provisional application Serial No. 60/190,233, filed March 17, 2000, which is hereby incorporated by reference.

Field of the Invention

This invention relates to methods for thermal processing of semiconductor wafers that contain a dopant material and, more particularly, to methods for achieving ultrashallow junctions in semiconductors wafers by the use of sub-melt laser annealing and low temperature rapid thermal annealing.

Background of the Invention

Ion implantation is a standard technique for introducing conductivity-altering dopant materials into semiconductor wafers. In a conventional ion implantation system, a desired dopant material is ionized in an ion source, the ions are accelerated to form an ion beam of prescribed energy, and the ion beam is directed at the surface of the wafer. The energetic ions in the ion beam penetrate into the bulk of the semiconductor material and are embedded into the crystalline lattice of the semiconductor material. Following ion implantation, the semiconductor wafer is annealed to activate the dopant material and to repair crystalline damage caused by the ion implantation. Annealing involves thermal processing of the semiconductor wafer according to a prescribed time and temperature protocol.

A well-known trend in the semiconductor industry is towards smaller, higher speed devices. In particular, both the lateral dimensions and the depths of features in semiconductor devices are decreasing. State of the art semiconductor devices require junction depths less than 1,000 angstroms and may eventually require junction depths on the order of 200 angstroms or less.

The implanted depth of the dopant material is determined by the energy of the ions implanted into the semiconductor wafer. Shallow junctions are obtained with low implant energies. However, the annealing process that is used for activation of the implanted dopant material causes the dopant material to diffuse from the implanted region of the semiconductor

wafer. As a result of such diffusion, junction depths are increased by annealing. To counteract the increase in junction depth produced by annealing, the implant energy may be decreased, so that a desired junction depth is obtained after annealing. This approach provides satisfactory results, except in the case of ultrashallow junctions. A limit is reached as to the junction depth that can be obtained by decreasing implant energy, due to the diffusion of the dopant material that occurs during annealing.

Numerous efforts have been made to develop annealing processes which limit diffusion of the dopant material, while achieving activation of the dopant material. Rapid thermal annealing or spike annealing is typically utilized when minimal thermal diffusion is desired. Rapid thermal annealing typically involves heating the wafer to a temperature of 950°C to 1100°C for a time of 1 to 30 seconds, whereas spike annealing may involve annealing times less than 0.1 second. Controlled, low concentrations of oxygen may be added to a nitrogen ambient to minimize thermal diffusion, as described in PCT Publication No. WO 99/39381. Notwithstanding careful selection of annealing parameters, rapid thermal anneals and spike anneals cause the dopant material to diffuse by thermal diffusion, transient enhanced diffusion, oxidation enhanced diffusion and dopant enhanced diffusion (i.e., boron enhanced diffusion or phosphorous enhanced diffusion). Even when low concentrations of oxygen are added to a nitrogen ambient and ultralow energy implants are performed, thermal diffusion still occurs.

Another known annealing technique is laser annealing, as described for example in U.S. Patent No. 5,908,307 issued June 1, 1999 to Talwar et al. and U.S. Patent No. 5,956,603 issued September 21, 1999 to Talwar et al. A surface layer of the wafer is amorphized, and a dopant material is implanted into the amorphized surface layer. The amorphized surface layer is then irradiated with laser energy sufficient to melt the amorphized surface layer, causing the dopant material to be distributed throughout the region of melted silicon. The integration of the laser annealing process with conventional device processes is relatively complicated. Silicon or germanium preamorphization implants are needed to avoid melting of the polysilicon gates, and deposition of an antireflective metal film is also necessary.

A technique for shallow junction formation by BF_2^+ ion implantation and excimer laser annealing with single pulse irradiation is described by H. Tsukamoto et al. in "Ultrashallow Junctions Formed by Excimer Laser Annealing," *Japanese Journal of Applied*

Physics, vol. 31, Pt. 2, No. 6A, 1992, pp. 659-662. The disclosed process produces high sheet resistance if the laser energy density is too low to cause melting.

U.S. Patent No. 4,151,008 issued April 24, 1979 to Kirkpatrick discloses thermal processing of selected regions of a semiconductor device with a short duration pulse of light from a pulsed laser or a flash lamp. The disclosed process produces high sheet resistance if light energy density is too low to cause melting.

All of the known prior art techniques for annealing semiconductor wafers have had one or more disadvantages, including, but not limited to, an unacceptable level of diffusion of the dopant material, high sheet resistance and excessive complexity. Accordingly, there is a need for improved methods for annealing semiconductor wafers which achieve the desired dopant distribution and sheet resistance, which repair crystalline damage, which minimize diffusion and which do not introduce excessive complexity into the fabrication process.

Summary of the Invention

According to a first aspect of the invention, a method is provided for thermal processing of a semiconductor wafer that contains a dopant material. The dopant material may be implanted or deposited in the wafer by ion implantation, plasma doping or any other suitable deposition technique. The method comprises the steps of irradiating the wafer with laser energy sufficient to activate the dopant material without melting the wafer and rapid thermal annealing of the wafer at relatively low temperature to repair crystalline damage.

Preferably, the step of irradiating the wafer with laser energy is sufficient to heat the wafer to a temperature in a range of about 1100°C to 1410°C, and the step of rapid thermal annealing of the wafer is sufficient to heat the wafer to a temperature in a range of about 650°C to 850°C for a time in a range of less than 1 second to 60 seconds.

The implanted wafer is preferably irradiated with laser energy having a wavelength in a range of about 190 to 1500 nanometers. In one embodiment, the implanted wafer is irradiated with laser energy having a wavelength of 308 nanometers. Other suitable laser wavelengths include 532 nanometers and 1064 nanometers. The laser energy used to irradiate the wafer may comprise one or more laser pulses. The wafer may be irradiated with laser energy comprising 100 to 1,000 laser pulses, and the pulse width of the laser pulses may be in a range of 10 to 100 nanoseconds. The product of the number of laser pulses times the pulse width of the laser pulses may be in a range of 1 to 1,000 microseconds. In one

embodiment, multiple laser pulses, each having a pulse width of about 20 nanoseconds, are used.

The laser anneal step may be performed in an ambient comprising oxygen in nitrogen, wherein oxygen concentration is controlled in a range of less than 1 to 1,000 parts per million during laser irradiation of the wafer. The rapid thermal annealing step may be performed in an ambient comprising oxygen in nitrogen, wherein oxygen concentration is controlled in a range of less than 1 to 1,000 parts per million during rapid thermal annealing of the wafer.

According to a second aspect of the invention, a method is provided for forming a doped region in a semiconductor wafer. The method comprises the steps of implanting a dopant material into the semiconductor wafer, irradiating the implanted wafer with laser energy sufficient to activate the dopant material without melting the wafer, and rapid thermal annealing of the implanted wafer at relatively low temperature to repair crystalline damage.

The method of the invention achieves dopant activation with no measurable diffusion. The rapid thermal anneal repairs crystalline damage from the implant of the dopant material, so that devices have good mobilities and low leakage currents. By eliminating melting of the silicon, dopant distribution throughout the melted region is avoided.

Brief Description of the Drawings

For a better understanding of the present invention, reference is made to the accompanying drawings, which are incorporated herein by reference and in which:

Fig. 1 is a simplified, partial cross-sectional view of a semiconductor wafer;

Fig. 2 is a flow chart that illustrates an embodiment of the process of the present invention; and

Fig. 3 is a graph of boron concentration in atoms per cubic centimeter as a function of depth in angstroms for different processes, including an embodiment of the process of the present invention.

Detailed Description

A highly simplified, partial cross-sectional view of a semiconductor wafer 10 is shown in Fig. 1. Junctions and regions of desired conductivities may be formed in the semiconductor wafer 10 by ion implantation. It will be understood that an actual semiconductor device includes multiple implanted regions in a complex configuration and

that the semiconductor device 10 of Fig. 1 is shown for illustrative purposes only. An ion beam 12 of a dopant material is directed at wafer 10, producing an implanted region 14. The depth of implanted region 14 is determined by a number of factors, including the energy and mass of the ions in ion beam 12. The boundaries of implanted region 14 are typically defined by an implant mask 16. The wafer is then annealed to activate the dopant material and to repair crystalline damage caused by ion implantation.

Prior art annealing processes have caused diffusion of the dopant material to an impurity region 20 that is larger and deeper than the implanted region 14. The impurity region 20 is characterized by a junction depth X_j, which is the depth of the impurity region 20 normal to the surface of wafer 10 after annealing. One of the goals in fabricating ultrashallow junctions is to minimize diffusion and to thereby limit the junction depth X_j.

It has been discovered that the junction depth X_j of impurity region 20 after annealing may be reduced in comparison with prior art processes by utilizing a novel thermal processing method including sub-melt laser annealing combined with low temperature rapid thermal annealing to form ultrashallow doped regions, with minimal thermal diffusion and without melting. The process can be used to form ultrashallow, low sheet resistance junctions and to form deeper impurity regions where thermal diffusion after ion implantation is undesired.

An embodiment of a process in accordance with the invention is shown in the flow chart of Fig. 2. A semiconductor wafer, typically a silicon wafer, may be implanted with a dopant material in step 50. Preferred dopant materials include, but are not limited to, boron, indium, arsenic, and phosphorous. In one example, boron is implanted at ultralow energy, i.e., an energy less than 1 keV. The dopant material may be implanted into the silicon wafer using a conventional ion implantation system, a plasma doping system or any other system capable of depositing or implanting the dopant material to a desired depth in the semiconductor wafer.

In step 52, the wafer containing the dopant material is irradiated with laser energy in a laser anneal step. The laser energy is sufficient to activate the dopant material without melting of the wafer. The wafer is placed in a laser anneal chamber having a controlled ambient and is irradiated with laser energy having predetermined parameters. The parameters of the laser anneal are selected to achieve a high wafer temperature, preferably in a range of about 1100°C to 1410°C, extremely rapidly without melting of the silicon or other

wafer material. Because the silicon is not melted, the laser anneal step is referred to as "sub-melt" laser annealing. The laser anneal step achieves dopant activation. Examples of suitable laser anneal parameters are described below.

Laser anneal step 52 preferably utilizes pulsed laser energy in a wavelength range of about 190 to 1500 nanometers. One preferred laser is an excimer laser having an output wavelength of 308 nanometers. Other suitable laser wavelengths include 532 nanometers and 1064 nanometers. Preferably, the laser energy should heat the silicon or other substrate material of the wafer to a depth of about 1 micrometer. Certain structures, such as polysilicon layers, are thermally isolated from the bulk silicon by a dielectric. When the laser energy is absorbed throughout a deep layer of bulk silicon, the thin polysilicon layer absorbs very little of that energy. It has been found that use of longer wavelengths in the above range prevents unwanted melting of the polysilicon gate.

The laser energy density used to irradiate the wafer is selected to heat a surface layer of the wafer rapidly, preferably in less than about 10 microseconds, to a temperature in the range of about 1100°C to 1410°C that does not melt the silicon. As known in the art, silicon melts at 1410°C. The laser energy density is preferably in a range of about 0.50 to 0.58 joules per square centimeter (J/cm^2) at a wavelength of 308 nanometers and a pulse width of 20 nanoseconds in order to achieve activation of the dopant material without melting of the silicon.

One or more laser pulses are preferably utilized to irradiate the wafer. The number of pulses may be in a range from 1 to 10,000, and the pulse width may be in a range of about 1 to 10,000 nanoseconds. The product of the number of laser pulses times the pulse width is preferably in a range from 1 to 1,000 microseconds. More preferably, the number of pulses is in a range of 100 to 1,000, and the pulse width is in a range of 10 to 100 nanoseconds. In one example of a suitable laser anneal, 100 pulses, each having a pulse width of 20 nanoseconds, are utilized to laser anneal a given area of the semiconductor wafer.

In one embodiment, laser anneal step 52 may be performed by a modification of a system used for conventional laser annealing wherein an amorphized layer of the wafer is melted. The parameters of the laser annealing system are modified to perform sub-melt laser annealing as described above. One suitable system is model LA-100 available from Verdant Technologies, which may be modified to perform sub-melt laser annealing as described above.

Depending on its cross-sectional area, the laser beam utilized to irradiate the wafer may cover the entire wafer area or a sub-area that is less than the entire area of the wafer. In one example, the laser beam has cross-sectional area of 10 millimeters by 10 millimeters at the wafer surface. Where the laser beam covers a sub-area of the wafer, the wafer may be stepped or scanned with respect to the laser beam in order to cover the entire area of the wafer. Thus, for example, a first sub-area of the wafer may be irradiated with 100 pulses, each having a pulse width of 20 nanoseconds, and then the wafer may be moved, or stepped, relative to the laser beam to a second sub-area, and the second sub-area may be irradiated with 100 laser pulses, each having a pulse width of 20 nanoseconds. This stepping process is repeated until the entire wafer area has been irradiated. Where the laser beam is sufficiently large to cover the entire wafer surface, a single sequence of laser pulses may be utilized to perform the laser anneal step. In another approach, the wafer may be stepped in small increments after one or more laser pulses, or it may be scanned continuously, so that the entire wafer surface receives the desired level of laser energy. In yet another approach, the wafer is held stationary, and the laser beam is deflected or otherwise moved relative to the stationary wafer in order to irradiate the entire wafer surface.

In step 54, the wafer is heated in a low temperature rapid thermal anneal step. The wafer is placed in a rapid thermal processing chamber having a controlled ambient and is heated according to predetermined parameters. The low temperature rapid thermal anneal is preferably in a temperature range of about 650°C to 850°C for a time in a range of less than 1 second to 60 seconds. The low temperature rapid thermal anneal repairs crystalline damage from the implant, so that the semiconductor devices have good mobilities and low leakage currents, but does not cause significant diffusion of the dopant material. In one example, the wafer is heated to 700°C for 20 seconds in the low temperature rapid thermal anneal step. Rapid thermal annealing systems for semiconductor wafers are commercially available. One suitable system is model AST-3000 available from STEAG-AST.

The low temperature rapid thermal anneal step 54 is shown in Fig. 2 as following the laser anneal 52. Alternatively, the low temperature rapid thermal anneal step 54 may be performed before laser anneal step 52.

The laser anneal step 52 may be performed in an enclosed chamber with a controlled ambient, preferably comprising oxygen in nitrogen at a pressure of one atmosphere. Preferably, the oxygen concentration in the laser anneal chamber is controlled during the

laser anneal step 52 in a range of less than 1 to 1,000 parts per million. The low temperature rapid thermal anneal step 54 may be performed in a thermal processing chamber with a controlled ambient, preferably comprising oxygen in nitrogen at a pressure of one atmosphere. In a preferred embodiment, the oxygen concentration in the thermal processing chamber is controlled during the low temperature rapid thermal anneal step 54 in a range of less than 1 to 1,000 parts per million.

The benefits of the thermal processing method of the invention are illustrated in the boron dopant profiles of Fig. 3. The dopant profiles shown in Fig. 3 were obtained by secondary ion mass spectrometry (SIMS). In Fig. 3, boron concentration in atoms per cubic centimeter is plotted as a function of depth from the wafer surface in angstroms for several different conditions. In each case, silicon wafers were implanted with boron (B^+) ions at an energy of 1 keV and a dose of 9E14/cm^2 (the notation 9E14/cm^2 represents an implant dose of 9×10^{14} atoms per square centimeter).

In Fig. 3, curve 70 represents a silicon wafer which was implanted with boron as described above, but was not annealed. Curve 72 represents a silicon wafer which was implanted with boron as described above and was spike annealed for a time of 0.2 second at a temperature of 1050°. Curve 74 represents a silicon wafer which was implanted with boron as described above and was rapid thermal annealed at 700°C for 20 seconds. The measured sheet resistance of this wafer was 3500 ohms per square. Curve 76 represents a silicon wafer which was implanted with boron as described above and was laser annealed below the melting threshold with 100 laser pulses at a wavelength of 308 nanometers, and then was rapid thermal annealed at 700°C for 20 seconds.

Curve 76 clearly shows that no measurable diffusion has occurred and yet a sheet resistance of 360 ohms per square has been produced. The junction depth at a concentration of 3E18/cm^3 in the wafer represented by curve 76 was 372 angstroms. By contrast, the wafer represented by curve 74 exhibited a much higher sheet resistance, indicating that the dopant material had not been activated. The spike annealed wafer represented by curve 72 exhibited significant diffusion of the dopant material, resulting in a junction depth of 561 angstroms. It will be understood that curves 70, 74 and 76 are nearly overlapping in Fig. 3.

The thermal processing technique described herein improves upon conventional high temperature rapid thermal annealing, either for a short time or a spike anneal, by only exposing the wafer to very high temperatures for a few microseconds, thereby minimizing

thermal diffusion of dopant materials. For the application of halo formation, this means that boron can be used as the dopant material instead of indium, which is presently used due to its lower diffusion but is not preferable since its source material is corrosive and leads to low ion source lifetimes. Another application of the disclosed process is the formation of source/drain extensions that are more abrupt than those formed by rapid thermal annealing. Source/drain extensions formed by this process have the abruptness of the as-implanted profile.

The invention also improves upon conventional laser annealing by eliminating melting of the silicon. This makes integration of the process into device process flows much easier and avoids dopant redistribution throughout the melted region. In addition, a preamorphizing implant is not required.

While there have been shown and described what are at present considered the preferred embodiments of the present invention, it will be obvious to those skilled in the art that various changes and modifications may be made therein without departing from the scope of the invention as defined by the appended claims.

CLAIMS

What is claimed is:

1. A method for thermal processing of a semiconductor wafer that contains a dopant material, comprising the steps of:

irradiating the wafer with laser energy sufficient to activate the dopant material without melting the wafer; and

rapid thermal annealing of the wafer at relatively low temperature to repair crystalline damage.

2. A method as defined in claim 1 wherein the step of irradiating the wafer with laser energy is sufficient to heat the wafer to a temperature in a range of about 1100°C to 1410°C.

3. A method as defined in claim 1 wherein the step of rapid thermal annealing of the wafer is sufficient to heat the wafer to a temperature in a range of about 650°C to 850°C for a time in a range of less than 1 second to 60 seconds.

4. A method as defined in claim 1 wherein the wafer is irradiated with laser energy from an excimer laser having a wavelength of 308 nanometers.

5. A method as defined in claim 1 wherein the wafer is irradiated with laser energy having a wavelength of 532 nanometers.

6. A method as defined in claim 1 wherein the wafer is irradiated with laser energy having a wavelength of 1064 nanometers.

7. A method as defined in claim 1 wherein the wafer is irradiated with laser energy having a wavelength in a range of about 190 to 1500 nanometers.

8. A method as defined in claim 1 wherein the wafer is irradiated with laser energy comprising a plurality of laser pulses.

9. A method as defined in claim 1 wherein the wafer is irradiated with laser energy comprising 1 to 10,000 laser pulses.

10. A method as defined in claim 1 wherein the wafer is irradiated with laser energy comprising laser pulses having a pulse width in a range of about 1 to 10,000 nanoseconds.

11. A method as defined in claim 1 wherein the wafer is irradiated with laser energy comprising 100 to 1000 laser pulses, and the pulse width of the laser pulses is in a range of 10 to 100 nanoseconds.

12. A method as defined in claim 1 wherein the wafer is irradiated with laser energy comprising one or more laser pulses and wherein the product of the number of laser pulses times the pulse width of the laser pulses is in a range of 1 to 1,000 microseconds.

13. A method as defined in claim 1 wherein the wafer is irradiated with laser energy comprising one or more laser pulses, each having a pulse width of about 20 nanoseconds.

14. A method as defined in claim 1 wherein a silicon wafer is irradiated with laser energy having an energy density in a range of about 0.50 to 0.58 J/cm^2 and a wavelength of 308 nanometers.

15. A method as defined in claim 1 wherein the step of rapid thermal annealing of the wafer has a duration of about 20 seconds.

16. A method as defined in claim 15 wherein the step of rapid thermal annealing of the wafer comprises heating the wafer to a temperature of about 700°C.

17. A method as defined in claim 1 wherein the step of rapid thermal annealing of the wafer is performed after the step of irradiating the wafer with laser energy.

18. A method as defined in claim 1 wherein the step of rapid thermal annealing of the wafer is performed before the step of irradiating the wafer with laser energy.

19. A method as defined in claim 1 further comprising the step of controlling oxygen concentration in a range of less than 1 to 1,000 parts per million during the step of irradiating the wafer with laser energy.

20. A method as defined in claim 1 further comprising the step of controlling oxygen concentration in a range of less than 1 to 1,000 parts per million during the step of rapid thermal annealing of the wafer.

21. A method for forming a doped region in a semiconductor wafer, comprising the steps of:

implanting a dopant material into the semiconductor wafer;

irradiating the implanted wafer with laser energy sufficient to activate the dopant material without melting the wafer; and

rapid thermal annealing of the implanted wafer at relatively low temperature to repair crystalline damage.

22. A method as defined in claim 21 wherein the step of implanting a dopant material into the semiconductor wafer comprises implanting boron at an energy less than 1 keV.

23. A method as defined in claim 21 wherein the step of implanting a dopant material into the semiconductor wafer comprises implanting a material selected from the group consisting of boron, indium, arsenic and phosphorous.

24. A method as defined in claim 21 wherein the step of irradiating the implanted wafer with laser energy is sufficient to heat the wafer to a temperature in a range of about 1100°C to 1410°C.

25. A method as defined in claim 24 wherein the step of rapid thermal annealing of the implanted wafer is sufficient to heat the wafer to a temperature in a range of about 650°C to 850°C for a time in a range of less than 1 second to 60 seconds.

26. A method as defined in claim 21 wherein the implanted wafer is irradiated with a plurality of laser pulses.

27. A method as defined in claim 21 wherein the implanted wafer is irradiated with laser energy having a wavelength in a range of about 190 to 1500 nanometers.

28. A method as defined in claim 21 wherein an implanted silicon wafer is irradiated with laser energy having an energy density in a range of about 0.50 to 0.58 J/cm^2 and a wavelength of 308 nanometers.

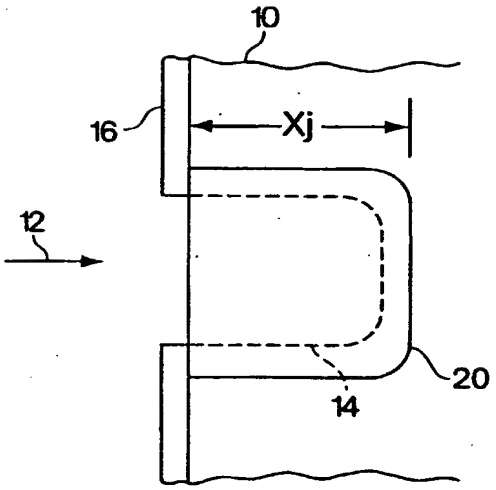

Fig. 1

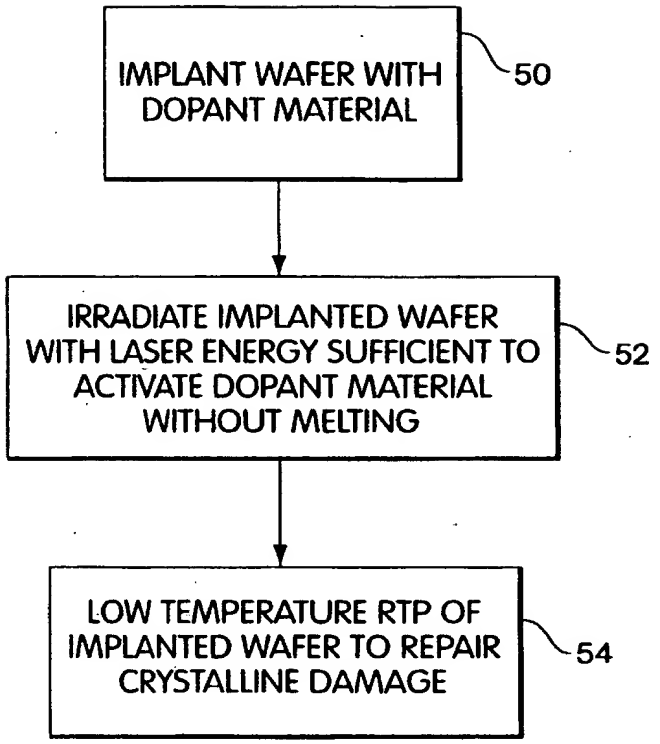

Fig. 2

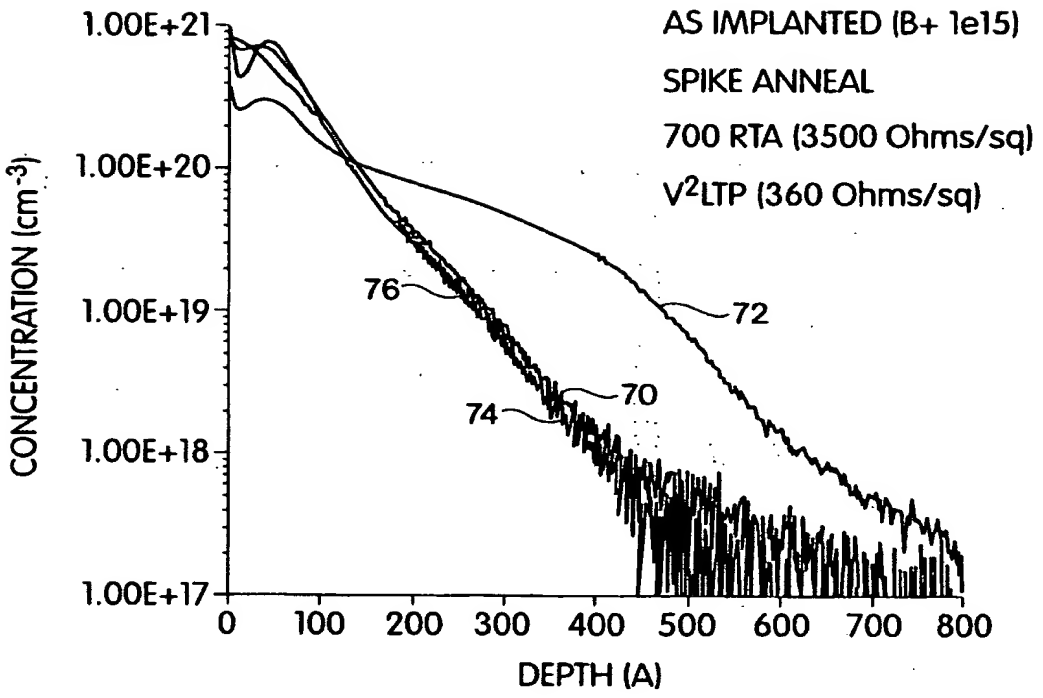

Fig. 3

INTERNATIONAL SEARCH REPORT

! ational Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/268 H01L21/265 H01L21/324

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 015, no. 070 (E-1035), 19 February 1991 (1991-02-19) -& JP 02 294027 A (SONY CORP), 5 December 1990 (1990-12-05)	1,4, 7-12,21, 26,27
Y	abstract	19,20,22
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A	column 3, line 35 -column 4, line 9; figure 3 column 6, line 51 - line 53	13,28

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

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Date of the actual completion of the international search	Date of mailing of the international search report
17 July 2001	24/07/2001

Name and mailing address of the ISA	Authorized officer
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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 01/08241

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 018, no. 277 (E-1554), 26 May 1994 (1994-05-26) -& JP 06 053157 A (SONY CORP), 25 February 1994 (1994-02-25) abstract	1,4,7,8, 10,13, 18,21, 23,26,27
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Form PCT/ISA/210 (continuation of second sheet) (July 1992)

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